

FIG.1
PRIOR ART

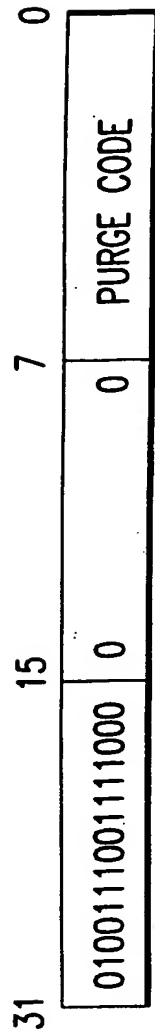


FIG.3A

PURGE CODE	PURGE DESIGNATION
0 0 X X X X X X	RESERVED
0 1 0 0 0 0 0 0	DATA SYSTEM MEMORY
1 0 0 0 0 0 0 0	INSTRUCTION SYSTEM MEMORY
1 1 1 1 1 1 1 1	ALL PURGE

X ... DON'T CARE

FIG.3B

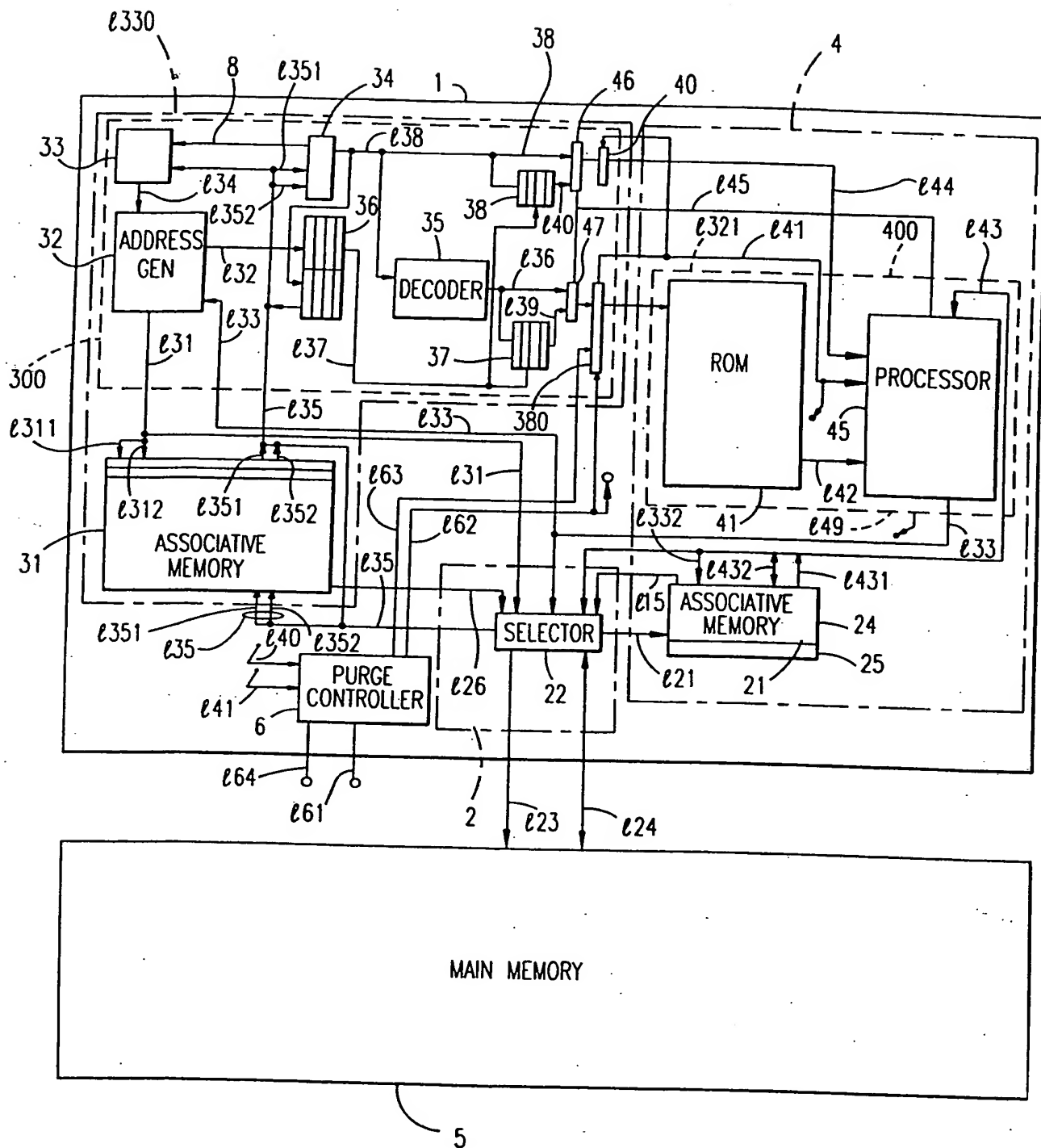


FIG.4

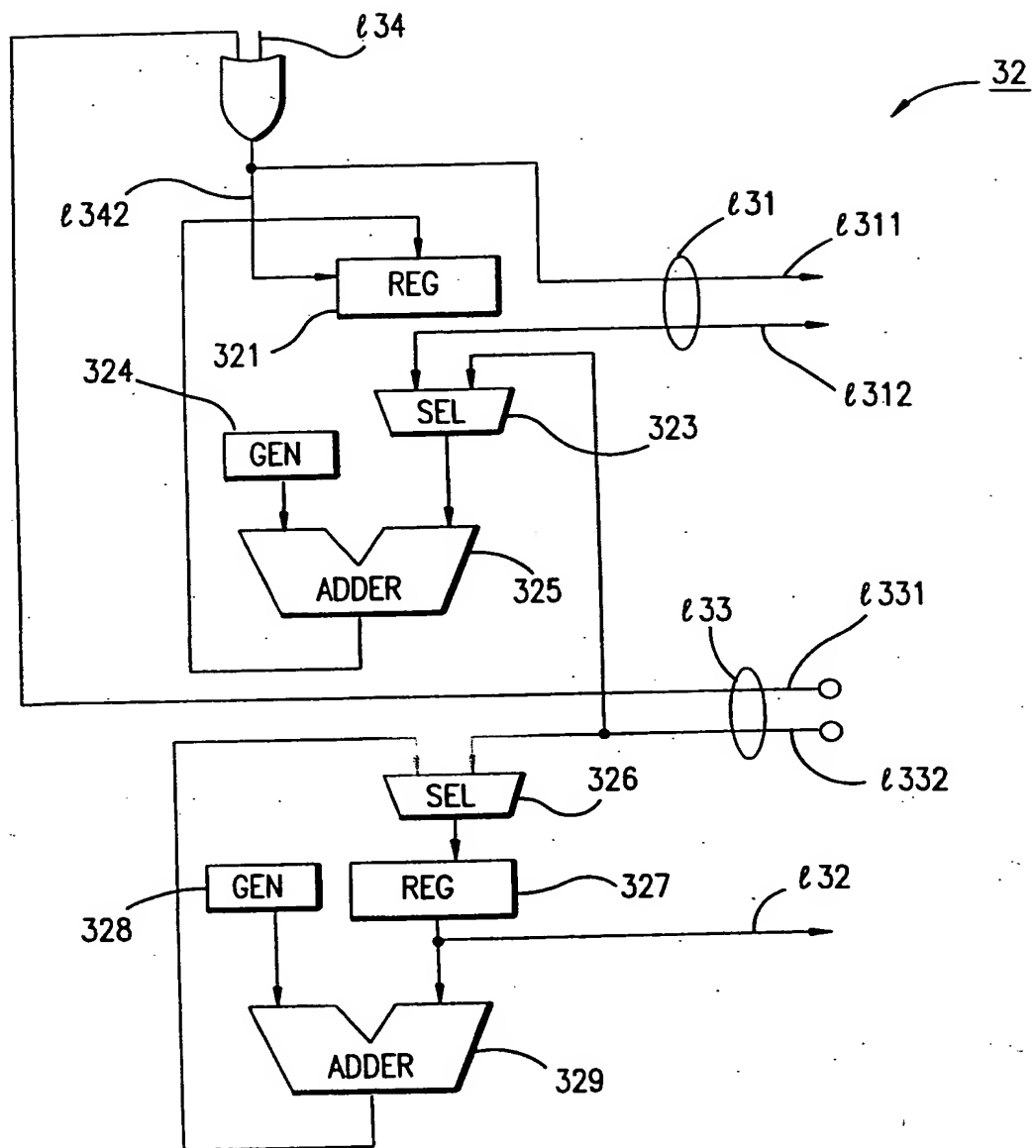


FIG.5

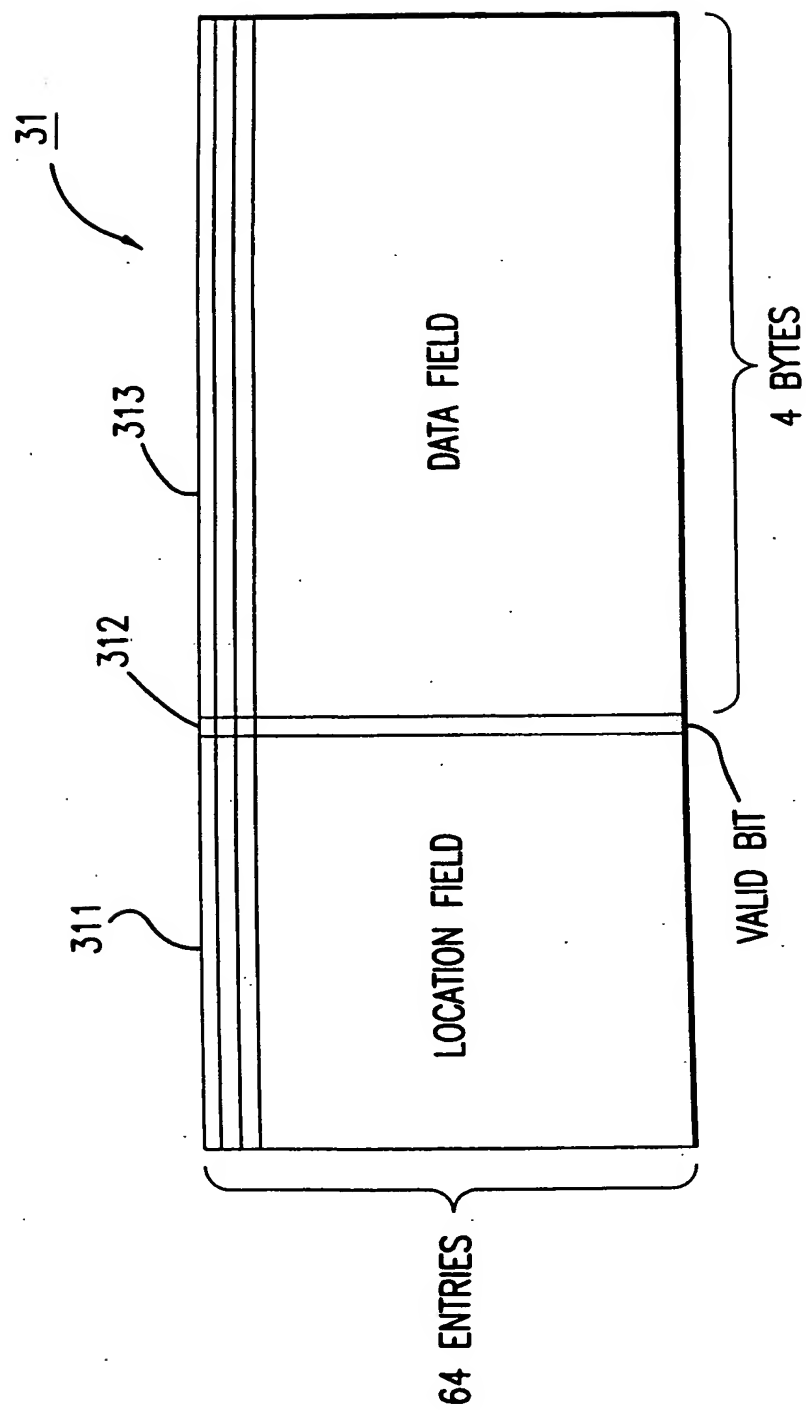


FIG.6

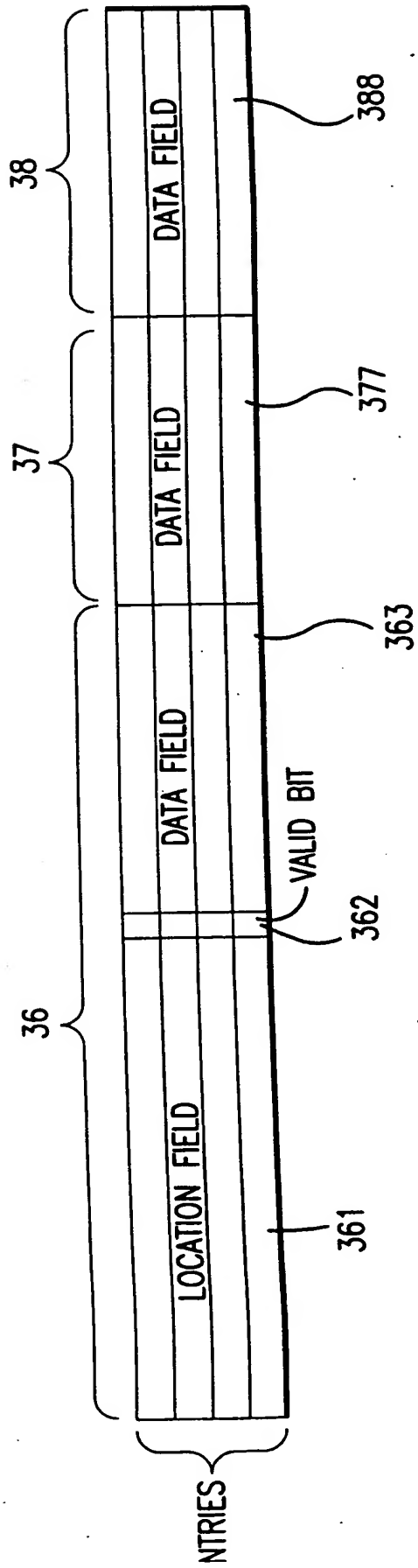


FIG.7

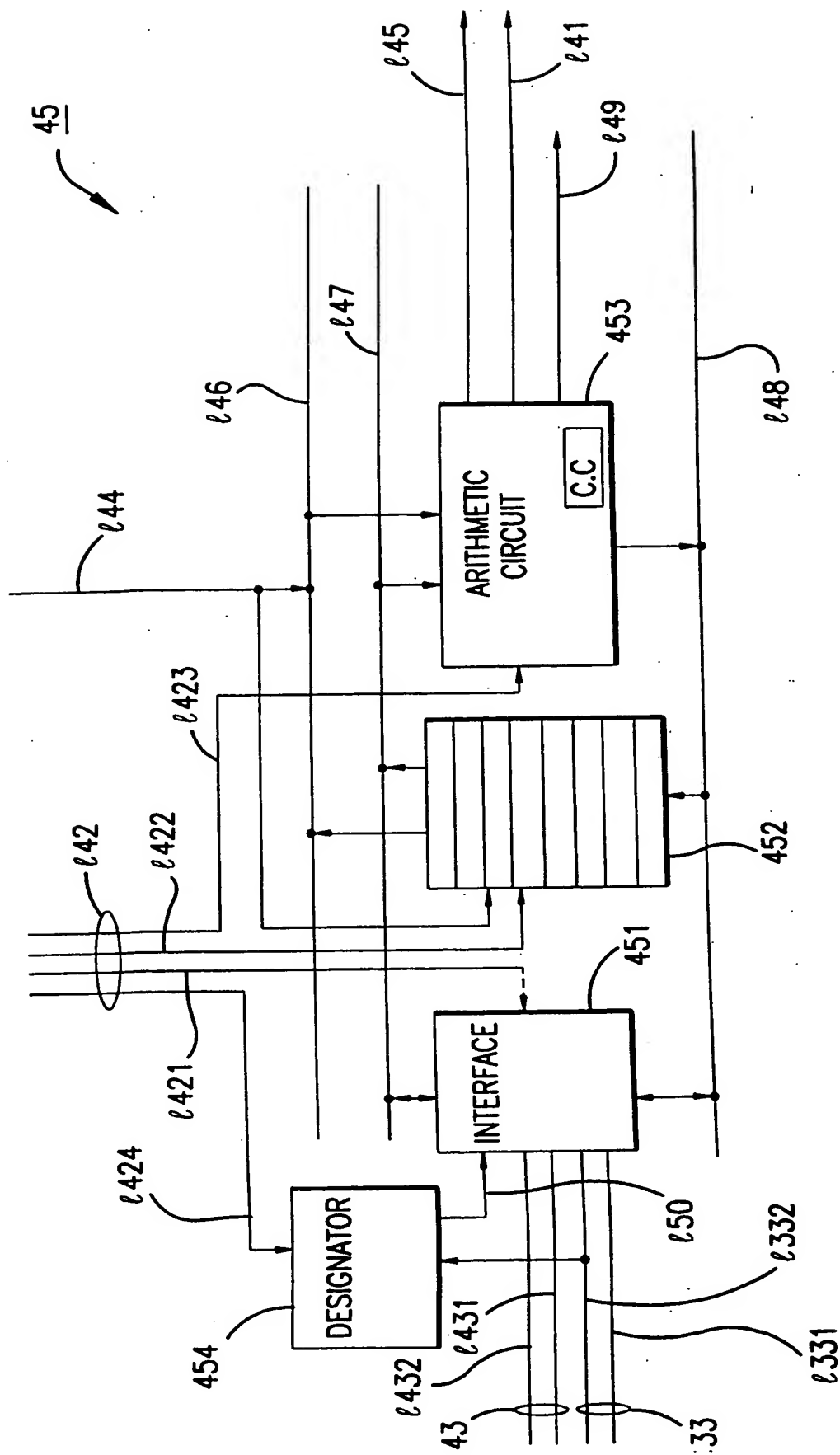


FIG.8

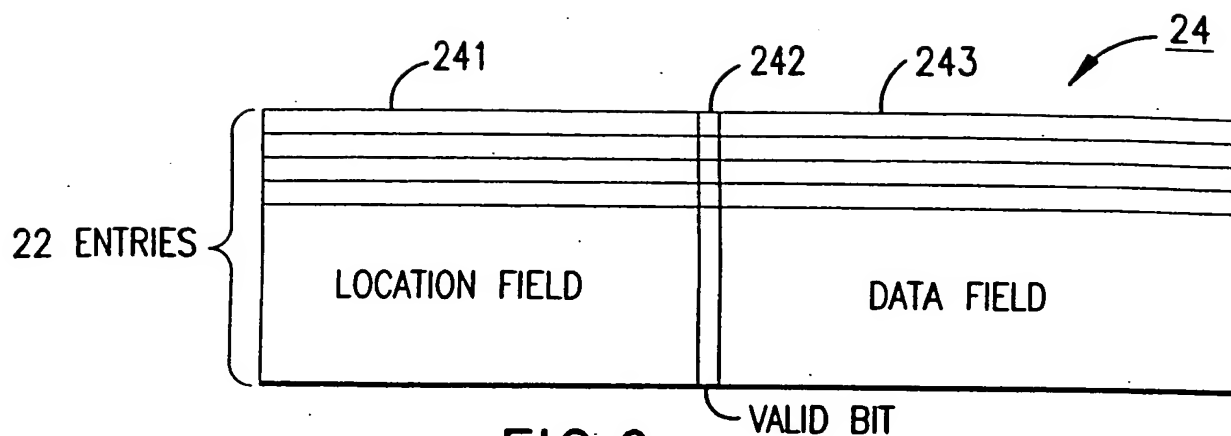


FIG. 9

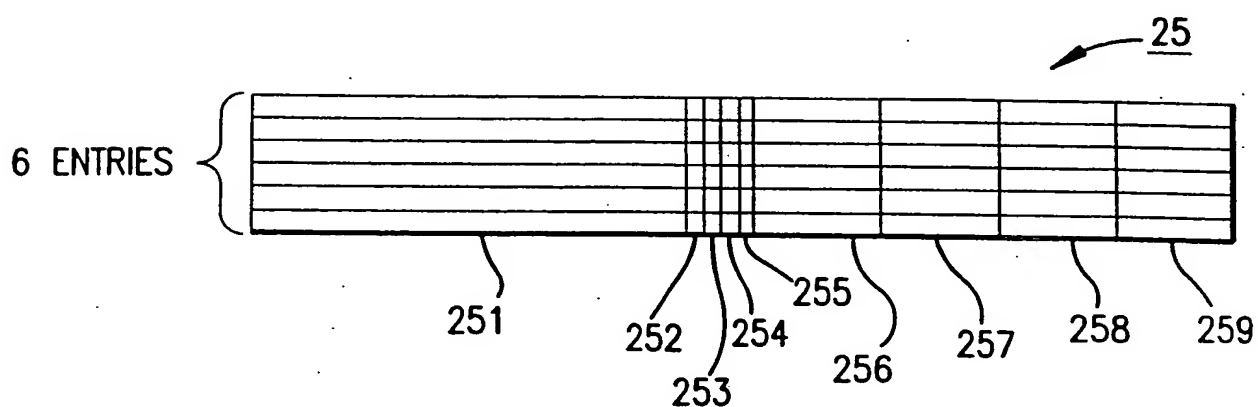


FIG. 10

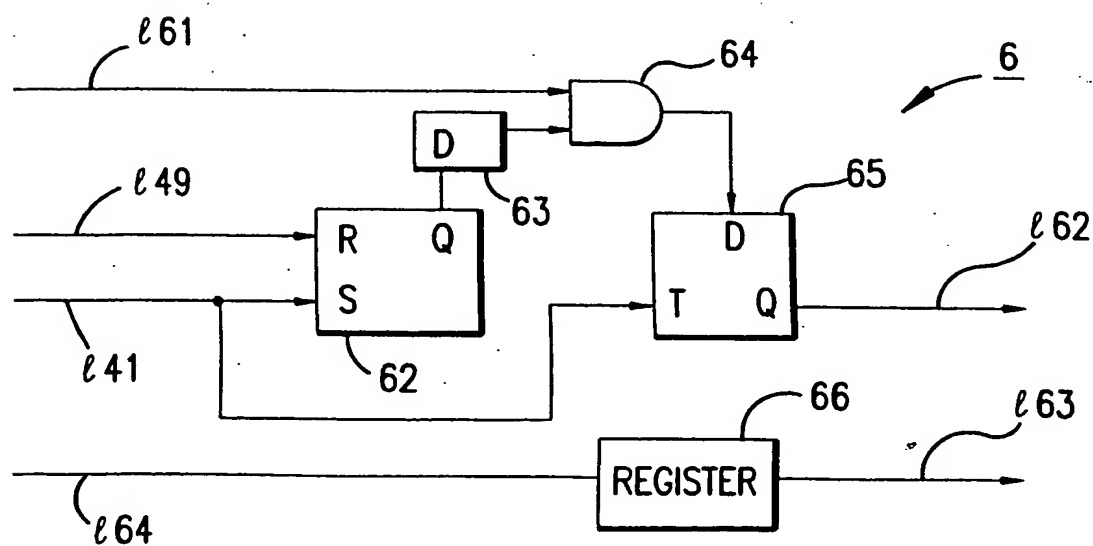


FIG 12

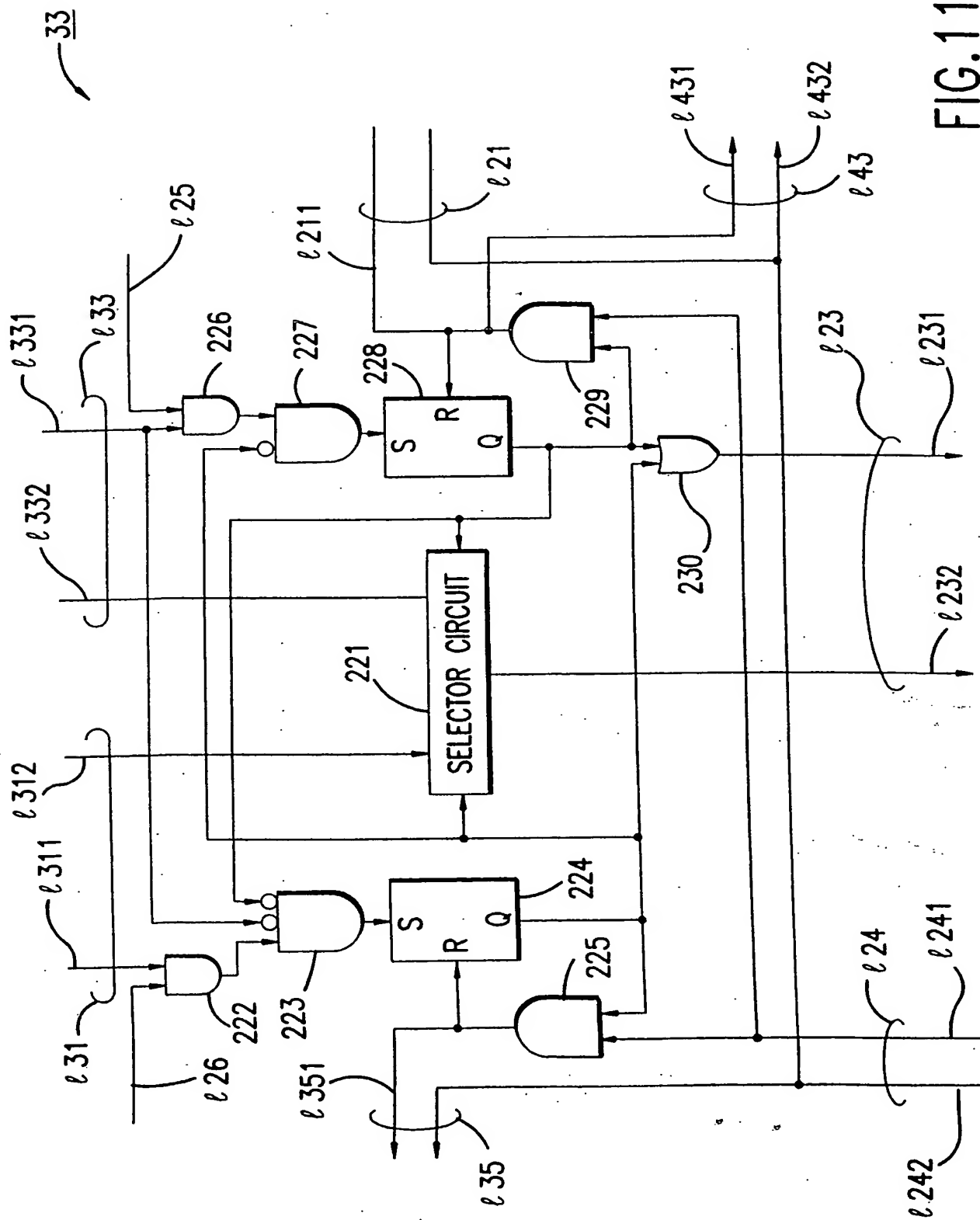
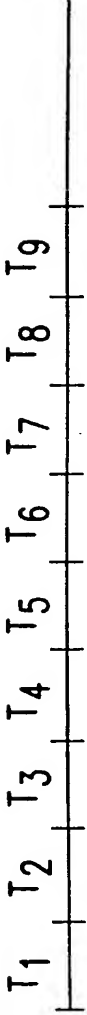


FIG. 11

NO.	ADDRESS MODES	PROCESS
NO.1	ADDRESS REGISTER INDIRECT	FETCH
NO.2	ADDRESS REGISTER INDIRECT	FETCH
NO.3	DATA REGISTER	ADD
NO.4	ADDRESS REGISTER	STORE
NO.5	ADDRESS REGISTER	JUMP TO NO.10
NO.6		
NO.7		
NO.8		
NO.9		
NO.10	DATA REGISTER	ADD
NO.11		

FIG.13



FETCH:

NO.1	NO.2	NO.3	NO.4	NO.5	NO.6	NO.7	NO.10	NO.11
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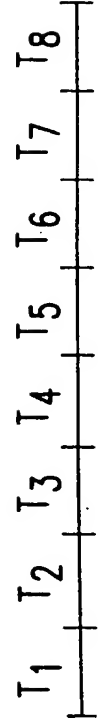
DECORD:

1	2	3	4	5	6	10
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EXECUTION:

NO.1	NO.2	NO.3	NO.4	NO.5	NO.10
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FIG.14A



FETCH:

NO.1	NO.2	NO.3	NO.4	NO.5	NO.6	NO.7	NO.12
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DECORD:

1	2	3	4	5	6	11
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EXECUTION:

NO.1	NO.2	NO.3	NO.4	NO.5	NO.10
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FIG.14B